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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,726	10/24/2001	Kenneth Y. Ogami	CYPR-CD01171M	2851

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,726	OGAMI ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-21* is/are allowed.

6)☒ Claim(s) *1-8,10 and 22-37* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/002,726 and communications filed on 3/21/2005. Claims 1-37 remain pending in the application and claims 38-41 are have been canceled as to non-elected claims.

Drawings

2. The informal drawings filed on 2/3/03 has been approved but contain poor quality. Accordingly, replacement drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to this Office action. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

3. New corrected drawings (Figs. 3-7E) in compliance with 37 CFR 1.121(d) are required in this application because the quality of drawings is poor. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 4-8, 10, 22-23, 25-31 and 33-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Barnett et al. (6,223,144).

6. As to claims 1, 22 and 30, Barnett et al. teach a microcontroller software tool for selecting available hardware configurations of hardware resources of a microcontroller for producing a modular configuration of selected hardware configurations and software development environments of a microcontroller by accessing a description of hardware resources of the microcontroller (Figs. 1B and 2 and its description; col. 5-6; Fig. 2A, target hardware model DLLs and software development environment DLLs). Barnett et al. teach that the microcontroller software testing tool comprises of a configuration core (configuration core of a microcontroller), and additional Dynamic Link Libraries that interface the tool to **selected hardware configurations** and software development environment (selected hardware configurations of microcontrollers or selected configurations of dynamically configurable blocks to produce a variety of functions) (col. 6 lines 6-18). Barnett et al. teach the software tool provides a modular configuration (configuration information) consisting of configurable core and additional Dynamic Link Libraries (DLLs) (available configurations of hardware resources of the microcontroller) (col. 4 lines 20-26; col. 6 lines 6-67). The user must specify the selected hardware configuration (produced selected configuration) and software development environment (col. 7 lines 3-14). The microcontroller software tool utilizes the specified hardware

configuration to selected the appropriate target hardware model DDL, shown in Figs. 2B and 2C. These teachings would explicitly show that Barnett et al. teach having available configurations of hardware resources of microcontroller to be selected to produce a selected configuration and generating configuration information corresponding to the selected configuration.

7. As to claims 2, 23 and 31, Barnett et al. teach the description of the hardware resources comprising a text readable data structure (col. 5-6; hardware description language description, standard document, see summary).

8. As to claims 4-5, 25-26 and 33-34, Barnett et al. teach selected configurations and software development environments to prove a modular configuration (col. 5-6) (read as predetermined configurations that are user modules to produce the selected configuration; Fig. 2C shows configuration of hardware resources as user modules; Figs. 2D shows data files location of predetermined configurations).

9. As to claims 6, 27 and 35, Barnett et al. teach the DLL contains all microcontroller specific information (instruction set) and hardware characteristic to configure a microcontroller (col. 6; Fig. 2B shows instruction set look-up table).

10. As to claim 7-8, 28-29 and 36-37, Barnett et al. teach application programming interface calls for embedded software (col. 5), wherein the application programming interface calls are named according to names given to configurations of the hardware resources (Figs. 2B-2D; for example naming sample in Fig. 2C and in file location naming also csample.sim; or csample.debug in Fig. 2D).

11. As to claim 10, Barnett et al. teach using microcontroller software testing tool for tracking the selected configuration (tracking the selected configuration and informing user) (col. 5-6) and informing the user if the selected configuration is achievable using the hardware resources is inherently included within the process because it is commonpractice during testing.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3, 24 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barnett et al. (6,223,144) in view of Zizzo (6,578,174).

14. As to claims 3, 24 and 32, Barnett et al. does not explicitly teach the text readable data structure is substantially compliant with extensible markup language (XML). Zizzo teaches a method and system for chip design using remotely located resources comprising circuit design platform to facilitate the design of an IC by making it easier for designers to locate and incorporate available virtual component blocks into new designs include using a universal data interface format or mark-up language (XML) is preferably used as a primary data interface between the various components of the system and the details XML are well-known to those in the art of computer programming (col. 7, 9). Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to implement the description of hardware resources with

extensible markup language (XML) because its universal data format, the XML language would be easy to implement and preferably used as primary data interface between various components (EDAs) of the design platform.

Allowable Subject Matter

15. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach or suggest generating an interrupt vector table for use by embedded software, wherein a plurality of interrupts included in the interrupt vector table are generated by the selected configuration along with a combination of based claims.

16. Claims 11-21 are allowed over the prior art of record. The prior art of record does not teach or suggest a combination of claimed limitations of accessing a description of dynamically configurable blocks that can be configured to produce a variety of functions; selecting available configurations of the dynamically configurable blocks to produce a selected configuration and generating configuration information corresponding to the selected configuration.

Remarks

17. Applicant(s) argued that Barnett et al. do not teach or suggest selecting available configurations of the hardware resources of said microcontroller. Examiner respectively submits that Barnett teach providing the microcontroller software testing tool comprises a configurable core (configurable microcontroller), additional dynamic link libraries

(DDLs) 210 and 220 (corresponding to configurable core of a microcontroller and additional dynamic link libraries read as available configurations) that interface the microcontroller software testing tool to **selected hardware configurations** (selected available configurations of the hardware resources of said microcontroller) and software development environments respectively to provide a modular microcontroller (generating configuration information corresponding to the selected configuration) (col. 6, lines 6-13). Thus, the teaching of **the selected hardware configurations** meet the claimed limitation of selecting available configurations of hardware resources of the microcontroller. The microcontroller software testing tool can support any microcontroller (also read as available hardware configurations to be selected) or any code development suite (col. 4 lines 20-26). Barnett et al. teach the microcontroller software testing tool provides a modular configuration (configuration information corresponding to the selected configuration) (col. 6 lines 58-59). Barnett et al. teach the user (designer) must specify the selected hardware configuration and software development environment. This clearly suggests having available configurations to be selected. The microcontroller software tool untilizes the specified hardware configuration to select the appropriate target hardware model DLL 210, shown in Figs. 2B and 2C (col. 6 lines 59-64). Since the claims do not recite what are the available configurations are referred to, Examiner believes that these teachings clearly suggest that Barnett et al. teach having available configurations of hardware resources of microcontroller to be selected to produce a selected configuration. The rejection under 103 is proper because Barnett teach a description of textual of an integrated circuit for

use to generate an integrated circuit (microcontroller and microprocessor) including testing and Zizzo teaches a description of an integrated circuit is extensible mark up language that is universal language for use in a circuit design. Therefore a combination of teachings would have been found obvious and proper to practitioners in the art because the extensible markup language is universal language and is easy to implemented and work equally as textual.

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER